A High Speed High Resolution Digital CMOS Sensor

Alex Krymski

Alexima, Pasadena, USA; krymski@alexima.com

This abstract is seeking a Poster slot at IISW'07 to report one of the two high speed high resolution sensors developed recently by the company. The first sensor is a 4.1Megapixel 400+ Frames/s shuttered CMOS sensor which is fully characterized. This chip delivers over 1.8 GPix/s of data at the maximum clock rate of 120 MHz. The other sensor has an anticipated data throughput of over 2 GPix/s and employs different array size, different readout architecture, and a high sensitivity pixel technology. However, this chip will only be tested in early March 2007, so the decision to disclose this chip to the Workshop can not be made at this time point, although the author would be willing very much to substitute the 4Meg described below with presenting of the more advanced sensor, should the new chip be fully tested by the time when the final manuscript is due AND should the new chip show good enough results from the first silicon.

The architecture of a 4Meg high speed sensor is based on column-parallel SAR ADCs and 4-quadrant symmetric readout as drawn in Fig.1. This shortens the length of internal memory bit lines and allows for an additional increase in speed. On the other hand, the layout-sensitive column ADCs are not divided into blocks, thereby giving no reason to possible block-readout FPN.

The pixel, the column amplifier, and the ADC are presented in Fig.2.

Fig.4 presents a minimally color-corrected JPEG-compressed image from the sensor and Table 1 summarizes the sensor performance.

The rest of the poster will discuss the T-5T- pixel in more details, the issues of distributing the controls and the clock of over the high speed chip, the row driver and the bias routing as a source of DSNU, and other design matters.

In the poster discussion, we'd like to share our experience on the following design topics to which the imaging design community does not have good answer yet:

- shall the pixel readout from a high speed sensor be differential?
- may the column circuit be unipolar, or shall it be differential or even fully differential?
- may we source the substrate of digital column circuits with an analog ground to reduce electronic noises?
- What is responsible for a hard reset pixel array shading: control distribution or bias distribution?

If the 4Meg chip is substituted with a new faster, over 2GPix/s digital CMOS sensor, then a new architecture, new pixel, and new data readout convention will be addressed.

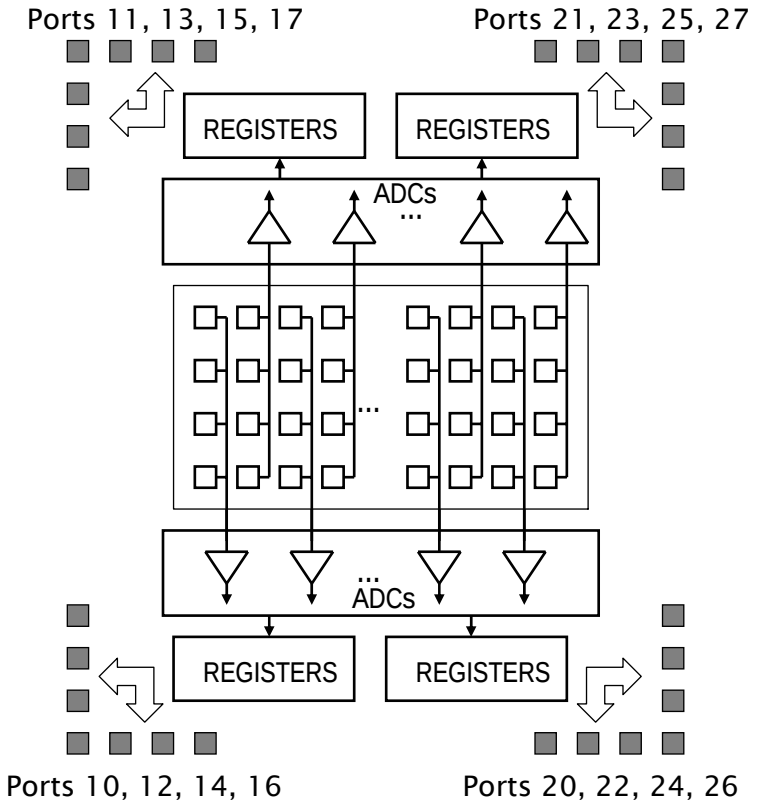

Fig.1. Readout architecture of the 4Meg sensor

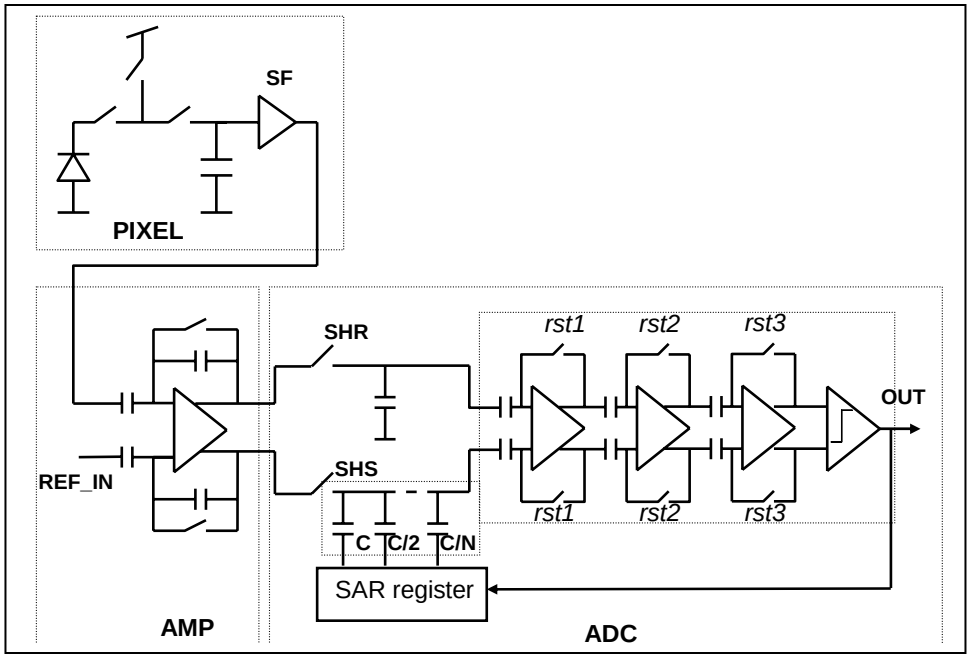

Fig.2. Pixel and Column simplified schematic

Fig.3. A sample picture taken with the 4M sensor, with minimum color correction

Table 1

Process	0.25um 1P4M
Array size	4.1Mpix, 2368x1728
Pixel	7um 5T shutter, T-type
Output	16 ports x 10 bit
Max clock rate	120 MHz
Max frame rate	440 Fps @ full resolution
Power	<1.5W
Full well/ noise	25,000e-/30e-
Responsivity	4V/Lux*s @550nm
DSNU	150e- rms