A 2 e^- Noise 1.3Megapixel CMOS Sensor

Alex Krymski, Nail Khaliullin, Howard Rhodes

Micron Imaging, Micron Technology, Inc.
135 N. Los Robles Ave, Pasadena CA, 91101

akrymski@micron.com

Abstract

Noise in the CMOS sensor with buried photodiode and column-parallel single-slope ADCs having a preamp is analyzed. A 1.3 Megapixel sensor built using such an architecture in 0.18um Micron CMOS sensor process sets up a new benchmark for CMOS sensors in noise: 1.5 electrons at the gain of 32.

I. Introduction

A new generation of CMOS sensors featuring a buried photodiode is being designed by key CMOS sensor manufacturers including Micron Technology, Inc. Gone are the times when CMOS sensors were blamed for dark current and dark sensitivity. Adopting the buried photo-detector technology has been critical in achieving low leakage and low photo-detector temporal noise. Yet, the design of the signal chain leaves some room for further optimization, performance improvement, and power reduction.

This paper addresses the low noise potential of a CMOS sensor with a buried photodiode and column-parallel ramp ADC architecture. CMOS sensors with such a detector were reported in [1-3], and the latter two, in particular, had a column-parallel ramp ADC. All three sensors had a sample-and-hold storage as the column input. One could calculate, that for the reasonable capacitor size and conversion gain, this would limit the sensor noise to approximately 3-5 e^- at best because of the storage kTC noise. The noise was 270 uV in [1], no noise data was given in [2], and a 340 uV or 14 electrons noise was reported in [3], which included an additional pixel source follower noise found in the CMOS process used.

In this paper we show that the sample and hold kTC noise can be suppressed in a column circuit with an amplifier prior to the sample and hold stage. In section II we consider sensor building blocks and the column readout schematic. Section III is devoted to the noise analysis of the signal chain. In Section IV, the results of the sensor characterization are presented followed by a picture taken from the sensor.

II. Sensor and column architecture

This sensor was designed to explore several readout and ADC architectures. The chip had two readouts from the pixel array, one in the bottom and one at the top of the pixel array (Fig.2.). The bottom readout was built of successive- approximation ADCs, with the major objective being the area reduction. This goal has been achieved, however, the performance of this column readout is beyond the scope of this paper. The top readout was of a ramp-ADC type with a preamp, both laid out column-wise. Each readout (bottom/top) had its own controller and memory arranged as parallel-in serial-out RAM. The memory/readout block was a minor redesign of the high-speed sensor readout [4].

One top readout column contained a switched-capacitor amplifier, a two-stage differential clocked comparator, and DRAM. A simplified schematic is presented in Fig.1.

The readout operates as follows. While the sensing floating diffusion (*FD*) of the 4T pixel is reset, the amplifier, the comparator, the ramp, and the ramp counter are reset as well. First, the pixel reset transistor *RST* gets open, then the amplifier feedback switch *rst_a* is released, and the comparator reset switches (*rc1, rc2)* are turned out one by one. One can notice, that the pixel reset kTC noise is stored in the amplifier input capacitor, the amplifier reset noise is stored in the first comparator input capacitor, and the first comparator reset noise is stored in its output pass capacitor. Since the noise from every previous stage is stored on a subsequent pass capacitor, it does not go through, and is thus cancelled. This is, basically, an extension of the well known correlated double sampling procedure over several consecutive readout stages. We can refer to

such a mechanism to as a "cascaded noise cancellation" or a "cascaded correlated double sampling ".

After the pixel reset and the sampling of the reset value is completed, the pixel transfer gate *TX* is made on and the photodiode charge is transferred into the floating diffusion. If the full charge transfer from the photodetector is achieved, there is no noise associated with the photodetector. This is one of the key advantages of having a buried photodiode detector. Voltage corresponding to the signal charge in the floating diffusion is then read out through the source follower *SF*, then gets amplified by the column amplifier, and then is stored in the sample and hold capacitor. This voltage is higher than the reset voltage from the amplifier output. During the ADC operation this voltage is compensated by a negative ramp voltage capacitively coupled to the storage. Simultaneously, the ramp counter is turned on. The Gray coded timing data is continuously refreshed in the DRAM and latched when the comparator flips. DRAM was chosen over other memories for its smaller input capacitance.

III. Noise sources

After cancellation of the reset noises described above, the remaining noises of the column readout are the source follower noise, the amplifier noise during the amplification, the sample-and-hold kTC noise (at least, for signal), and ADC noises. In estimating these noises for our design, we will compare two situations: the unity gain, and the gain of 8.

The source follower noise comes as the thermal noise from the pixel source follower and from the current sink. These two noises are represented respectively as the equivalent voltage source and the current source in Fig.3. Typically, the amplifier bandwidth in unity gain (reset) configuration is higher than that of the source follower, but smaller in the high gain mode. This is dictated by amplifier power optimization. The source follower stage noise transforms into kTC noise for pixel reset phase, where the capacitance includes the pixel array column readout capacitance and the amplifier input capacitance (1pF, and 0.5pF, respectively). In the amplification phase, the source follower noise is filtered out by amplifier with smaller bandwidth. 1/f noise of the source follower MOSFET was estimated to be 15 uV.

In order to calculate the amplifier noises, one needs to resolve the equations following from the small-signal equivalent circuit for the amplifier stage (Fig.4.). Ignoring the contribution from the amplifier reset, which is cancelled by the comparator, the amplifier noise at output during the amplification can be reduced to the following simple formula (Fig.4. right), which breaks into easy explainable pieces. One can see that this is a kTC-type noise with the capacitance the total output amplifier capacitance [load capacitor plus feedback and input capacitors in series]. The noise also includes the square of gain (assuming the amplification of the amplifier g_m–defined input thermal noise). Another gain factor in the denominator represents a linear amp stage bandwidth reduction with gain. This noise is then referenced to the pixel by dividing it by the amplifier gain (Cin/Cfb) and the pixel conversion gain of 0.85 (HSPICE-simulated).

The next noise is the sample/hold kTC noise. During the reset phase the comparator feedback switch is closed, so the storage capacitance is made of 2 capacitors and is 1 pF. During amplification, one capacitor becomes floating, and the capacitance becomes 0.5 pF.

ADC quantization noise is 1LSB/ $12^{1/2}$, where LSB stays for "least significant bit".

We disregard the comparator noise here, because it is partially cancelled, and contributes post-gain and thus is not critical for the case of high amp gain, our scope here.

All calculated noises are summarized in Table.1. Using the circuit with amp and ramp ADC, pixel noise of less than 100 uV can be reached even with relatively small (0.5 pF) column capacitors.

IV. Measurement results.

The sensor was designed and fabricated in 0.18um CMOS sensor process recently developed by Micron Technology, Inc. The characterization bench included custom board with USB-2 link to PC, Davidson light source with set of filters, custom data acquisition and characterization software.

Figure 5 is a plot of the typical pixel leakage vs. temperature obtained from one of the new Micron Imaging products. It shows that dark current is very low for the process developed. Figures 6, 7, and 8 represent some of the measurement data obtained from the reported sensor. These include the plots of the sensor responsivity, ADC differential nonlinearity (DNL), and histograms of the response to demonstrate the uniformity of column readout

circuits. The experimental data is summarized in Table 2.

The amplifier had fixed gains of 1,2,4, and 8. Additional gain could be enabled by the lowering of ramp ADC voltage. For example, when we report gain of 32, it included the amplifier gain of 8 and the ramp ADC voltage of 250 mV instead of the nominal 1V.

Normally the sensor is operated at 30 Frames/s with 50 mW power (no internal biases on the chip which would add 20-30% power). At this frame rate the sensor noise was quite small but still dominated by electronic noise. For the purposes of minimizing this noise, the sensor was turned into the mode when the readout did not overlap with row operations and ADC, and the frame rate was reduced. The noise of 1.5 electrons was measured at 6 frames/s, the maximum amplifier gain of 8, and the ramp ADC gain of 4 (250 mW ADC reference). In the overlapped readout mode the noise was higher. For example, a 4.4 e^- was measured at 30 Fps and gain of 8. Row-wise electronic noise contributed 4.1 e^-. After subtracting this noise which correlated in rows, the remaining random noise component was 1.7 e^-. We believe that a proper design of biases on-chip will allow us to cancel this row noise in future designs.

The paper is concluded with an image obtained in low light conditions (Fig.9).

V. Summary

A CMOS sensor with noise of 1.5 electrons has been designed and demonstrated. We believe that this was the lowest noise CMOS sensor (of a consumer-type resolution/ pixel size) reported so far. The low noise readout scheme included a buried photodiode in the pixel, an amplifier prior to the storage capacitors and 2-stage comparator in the column, and featured a cascaded noise cancellation. The noise analysis carried in the paper can be used for noise reduction in future designs. For instance, the column current sink noise ideally should not be present. Only a little effort is needed to reach the noise limit of 1 electron and thus turn the sensor into a photon counting mode. Higher pixel conversion gain would also be a help in reducing sensor noises expressed in electrons, if the pixel saturation is not a concern.

VI. Acknowledgement

Authors would like to acknowledge contribution of Nianrong Tu, Nikolai Bock, Marilyn Sutanu and Aleksandr Sevastyanov to this project, and would like to thank Parker Altice and Don Robinson for providing a “hot” dark current temperature data from one of the newly tested products.

References

1. S. Inoue et al., “ A 3.25 M-pixel APS-C size CMOS Image Sensor”, 2001 Workshop on CCDs and AIS, 2001, Tahoe, pp. 16-19.
2. T. Sugiki et al., “A 60 mW 10b CMOS Image Sensor with Column-to-column FPN Reduction”, Proceedings of ISSCC, 2000, pp.108-109.
3. K. Findlater et.al., “SXGA Pinned Photodiode CMOS Image Sensor in 0.35um Technology” Proceedings of ISSCC, 2003, pp218-219.
4. A. Krymski et.al “A High Speed, 500 Frames/s, 1024x1024 CMOS Active Pixel Sensor”, 1999 VLSI Circuits Symposium, Kyoto, 1999, pp. 137-138.

Table 1. Calculated signal chain noises

	Gain=1	Gain=8
Pixel SF Noise	97uV	74uV
Amp Noise	116uV	31uV
S&H Noise	130uV	16uV
Subtotal Noise uV or e^- @ 60uV/e	200uV or 3.3 e^-	82uVor 1.4e^-
ADC Noise @1V	270uV	-
Total Noise, e^- @ 60uV/e	340uV or 6e^-	82uV or 1.4e^-

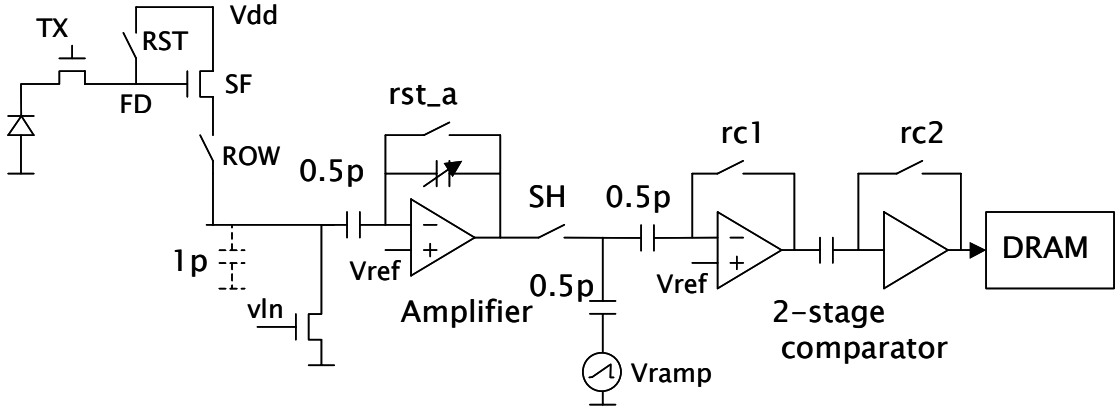


Fig.1. Block- schematic of pixel and one column readout

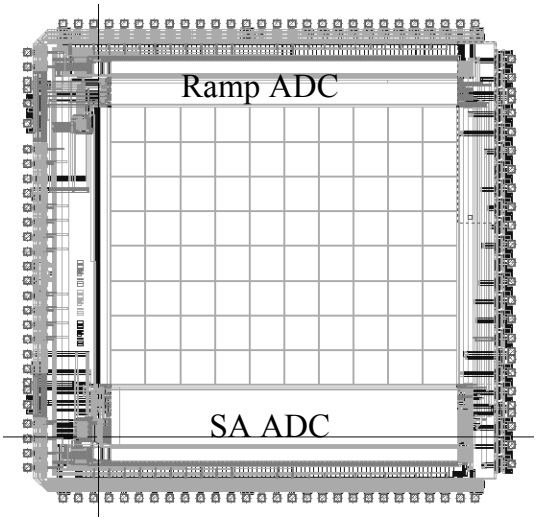
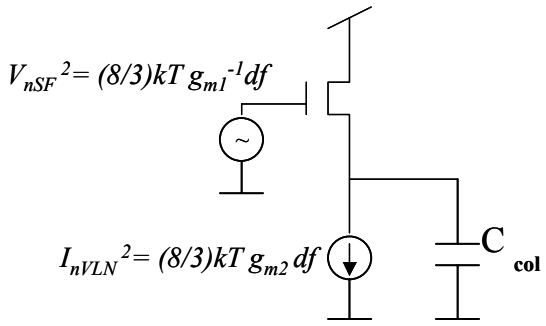
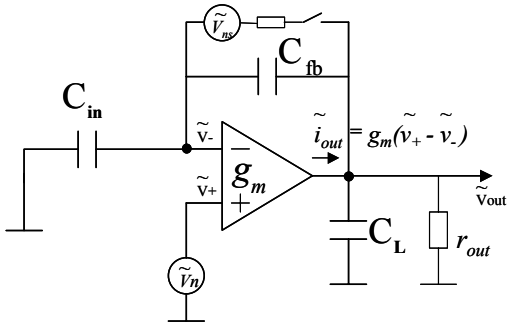


Fig.2.The chip layout.



$V_{SF}^2 = (2/3)kT/C_{col}\,(1+g_{m2}/g_{m1})$ (if kTC-noise bandwidth is not limited by subsequent amp stage)

Fig.3. Noise of the pixel source follower



$$\overline{\tilde{v}_{outs\_n}^2} = \frac{2}{3}\,kT\,\frac{(C_{in}+C_{fb})^2}{C_{fb}^2 C_{in} + C_{fb}(C_{fb}+C_{in})C_L} =$$

$$= \frac{2}{3}\,kT\,\underbrace{\frac{1}{C_L + C_{fb}C_{in}/(C_{fb}+C_L)}}_{\text{output capacitance}}\underbrace{\left[\frac{C_{fb}+C_{in}}{C_{fb}}\right]^{-1}\left[\frac{C_{fb}+C_{in}}{C_{fb}}\right]^{2}}_{\text{gain (for in+)}}$$

$v_{out}^2 = gain^2\,(8/3)kT\,g_m^{-1} df;\ df \sim 1/(g_m^{-1} C_{out} * gain)$

Fig.4. Equivalent circuit for amplifier noise (left) and the noise in the amplification phase (the amplifier reset noise assumed cancelled)

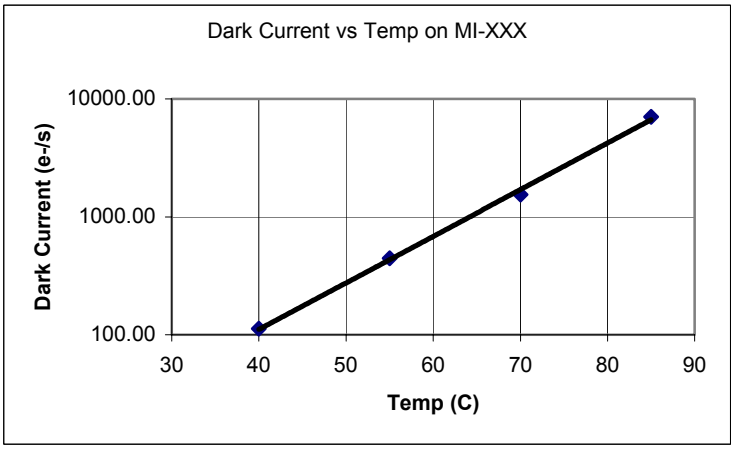


Fig.5. Dark current vs. temperature data for new 0.18um Micron CMOS sensor process. Pixel size is ~5um

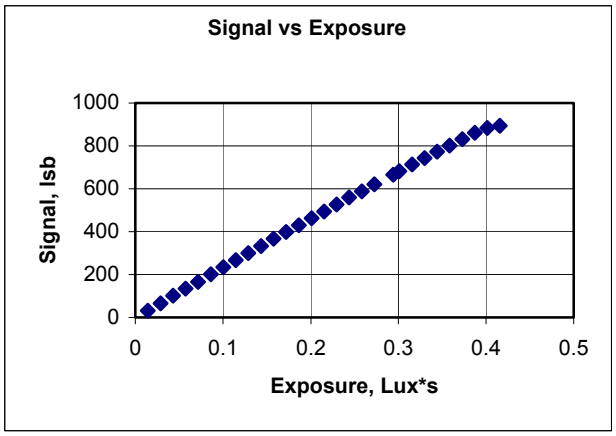


Fig.6. Digital responsivity plot.

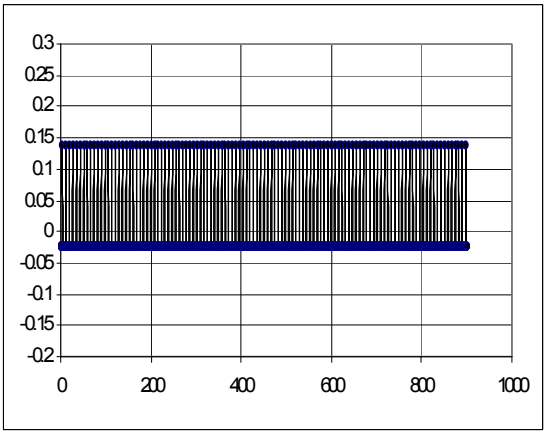
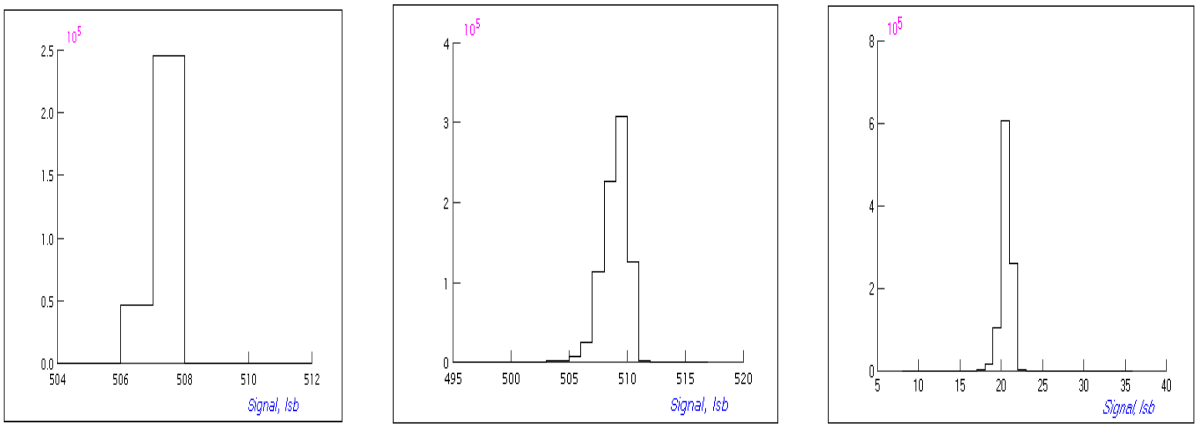


Fig.7. ADC DNL (in lsb vs. code)



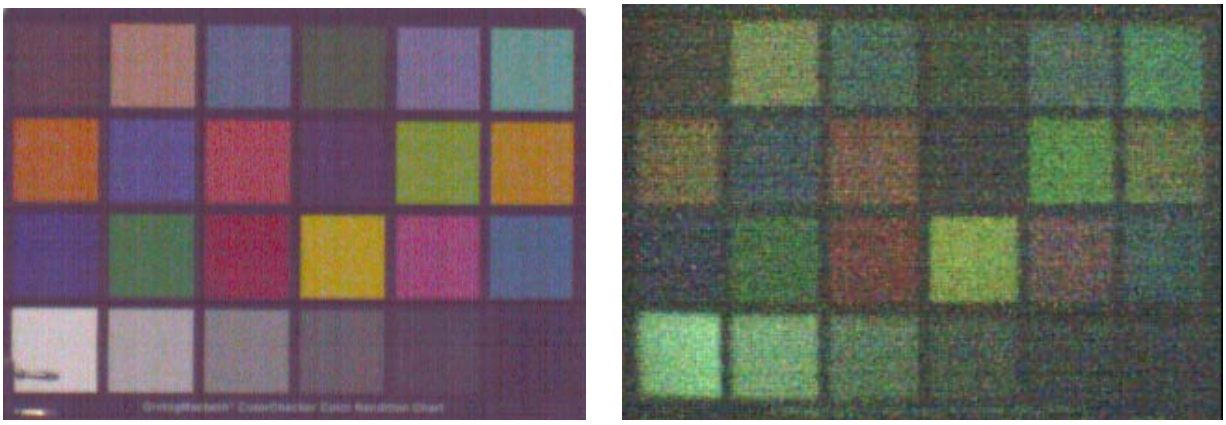
a b c

Fig.8. Histograms taken a) with electrical input to column, gain=1, ~510 lsb; b) electrical input, gain=8, ~510 lsb; c) optical input, gain=8, ~20 lsb;

Table 2. Sensor parameters

Technology	0.18um 2P3M CMOS Sensor
Color	RGB
Pixel	3.9um 4T buried photodiode
Format	1280x1024
Power	50 mW @ 3.3V @30 Fps (no biases on the chip)
Frame rate	30 Frames/s
Noise	$8e^-$ @ 30 Fps, gain=1; 4.4 e^- @ 30 Fps, gain=8; 1.5e^- @ 6 Fps, gain=32**
Quantum efficiency	50% @550 nm, CFA + u-lenses
Saturation	14,000 e- @ gain=1; V_{ADC}=1V
Pixel conversion gain	0.064 lsb/e- @ gain=1; V_{ADC}=1V
Maximum SNR	42 dB
DSNU	0.5 lsb rms or 0.05% sat (gain=1); 1.2 lsb rms (gain =8)
Column fpn	0.2 lsb rms (gain=1; dark); 0.45 lsb rms (gain=8; dark)
Dark current	<60 lsb/s @ 60^o C
PRNU	7 lsb rms or 1.5% at ½ saturation, gain=1
Responsivity	2.1 V/Lux*s
ADC	Column parallel, ramp 10b
ADC INL, DNL	<0.5 lsb p-p

** Gain 32 included amplifier gain of 8 and ramp ADC gain of 4.



Reported sensor
Illuminance : 1 lux;
Integration time: 167 ms (6 fps)
Pixel: 3.9um

Competition sensor with pinned diode
Illuminance: 5 lux;
Integration time: 33.3 ms (30 fps);
Pixel: >5 um

Fig.9. Raw color image taken at low light. Window close to CIF format was selected for reported sensor. Aperture and exposure were the same for both sensors.